## VI Semester

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Subject Code</th>
<th>Subject</th>
<th>Credits</th>
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<tbody>
<tr>
<td>1</td>
<td>UEC611C</td>
<td>Field Theory</td>
<td>4.0</td>
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<tr>
<td>2</td>
<td>UEC612C</td>
<td>Computer Networks</td>
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<tr>
<td>3</td>
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<td>Information Theory and Coding</td>
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<td>4</td>
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<td>CMOS Digital VLSI Design</td>
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<tr>
<td>5</td>
<td>UECXXXE</td>
<td>Elective-III</td>
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<tr>
<td>6</td>
<td>UECXXXE</td>
<td>Elective-IV</td>
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<tr>
<td>7</td>
<td>UEC621L</td>
<td>Computer Network Lab</td>
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<td>8</td>
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<td>VLSI Lab</td>
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### Elective-III

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<tr>
<td>1</td>
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<td>Bio Medical Engineering</td>
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<td>2</td>
<td>UEC616E</td>
<td>Operating System</td>
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<tr>
<td>3</td>
<td>UEC617E</td>
<td>Advanced Microprocessors</td>
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### Elective-IV

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<tr>
<td>1</td>
<td>UEC618E</td>
<td>Applications of Signal Processing</td>
<td>3.0</td>
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<tr>
<td>2</td>
<td>UEC619E</td>
<td>DSP Processors</td>
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<td>3</td>
<td>UEC620E</td>
<td>Mobile Communication</td>
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</table>
Course Title: Field Theory

Course Code: UEC611C

Credits: 4
Teaching Hours: 52 Hrs (13 Hrs/Unit)
Contact Hours: 4 Hrs/Week

CIE Marks: 50
SEE Marks: 50
Total Marks: 100

Unit I

Vector analysis, Coulomb’s Law and electric field intensity: Experimental law of coulomb, coulomb’s law, field intensity, field due to continuous volume charge distribution, Field of a line charge & field of sheet charge, field of a volume charge, Electric flux density. Gauss law and divergence: Electric flux density, Gauss law, Application of Gauss law to symmetrical charge distribution & differential volume element, Divergence Maxwell’s first equation, vector operator del and divergence theorem.

Unit II

Energy and potential: Energy expended in moving a point charge in an electric filed, the line integral, definition of potential difference and potential, the potential filed of a point charge and system of charges, potential gradient, Energy density in an Electrostatics filed. Conductors, dielectrics and capacitance: Current and current density, continuity of current, metallic conductors, conductor properties and boundary conditions, boundary conditions for perfect dielectrics, capacitance and examples.

Unit III


Unit IV

Time varying fields and Maxwell’s equations: Faraday’s law, displacement current, Maxwell’s equation in point and integral form, retarded potentials. Uniform plane wave: Wave propagation in free space and dielectrics, poynting’s theorem and wave power, propagation in good conductors (skin effect), wave polarization. Plane wave in boundaries and in dispersive media: Reflection of uniform plane waves at normal incidence, SWR, wave reflection from multiple interfaces, plane wave propagation in general directions.

Text Book:

**Reference Books:**

<table>
<thead>
<tr>
<th>Course Title: Computer Networks</th>
<th>Course Code: UEC612C</th>
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<td>Credits: 4</td>
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**Unit I**


**Unit II**

Multiple Access: Random access, Controlled access, Channelisation, Wired LAN, Ethernet, IEEE standards, Standard Ethernet. Changes in the standards, Fast Ethernet, Gigabit Ethernet, Wireless LAN IEEE 802.11, Connecting LANs, Backbone and Virtual LANs, Connecting devices, Backbone Networks, Virtual LANs.

**Unit III**

Network Layer, Logical addressing, Ipv4 addresses, Ipv6 addresses, Ipv4 and Ipv6 Transition from Ipv4 to Ipv6, Delivery, Forwarding, Unicast Routing Protocols, Multicast Routing protocols.

**Unit IV**

Transport layer Process to process Delivery, UDP, TCP, Application Layer: Domain name system, Name Space, Domain Name Space, Distribution of Name Space, DNS in the Internet, Resolution, DNS messages, Types of Records, Registrars, Dynamic Domain Name System, Encapsulation.

**Text Book:**


**Reference Books:**

Unit I


Unit II

Communication channels: Discrete communication channels, Entropy functions and equivocation, Mutual information, Properties of mutual information, Rate of information transmission over a discrete channel, Capacity of a discrete memory less channel, Shannon’s theorem on channel capacity, Channel efficiency and Redundancy. Special channels: Symmetric/Uniform channels, Binary symmetric channels, Binary erasure channel, Noiseless channel, Deterministic channel. Discrete channels with memory. Continuous Channels: Differential entropy and Mutual information for continuous ensembles, Shannon-Hartley law and its implications.

Unit III


Unit IV


Text Books:

Reference Book:

<table>
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<tr>
<th>Course Title: CMOS Digital VLSI Design</th>
<th>Course Code: UEC614C</th>
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### Unit I


### Unit II


### Unit III


### Unit IV


### Text Book:


### Reference Books:

1) Jan M.Rabaey, Anantha Chandrakasan, Borivoje Nikolic, “Digital Integrated Circuits A
Design Perspective” Pearson Education Publisher, 2nd Edition.
Unit I


Unit II

Electrocardiograph: Electrical activity of the heart, characteristics of electrocardiogram (ECG), block diagram description of an electrocardiograph, ECG lead system, multi-channel ECG machine. ECG signal processing aspects. Cardiac pacemakers: Need for cardiac pacemaker, external pacemaker, implantable pacemaker, programmable pacemaker, rate responsive pacemakers. Defibrillators: AC & DC defibrillators. Electroencephalograph: Genesis of electroencephalogram (EEG), block diagram description of an electroencephalograph, 10-20 electrode systems, and computerized analysis of EEG. Electromyograph.

Unit III


Unit IV


Text Books:
1) Leslie Cromwell, Fred J Weibell, Erich A. Pfeiffer, “Biomedical Instrumentation and Measurements”, PHI, 1999

**Reference Books:**

<table>
<thead>
<tr>
<th>Course Title: Operating Systems</th>
<th>Course Code: UEC616E</th>
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<td>Total Marks: 100</td>
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**Unit I**

Introduction and Overview of Operating Systems: Operating system, Goals of an O.S, Operation of an O.S, Resource allocation and related functions, User interface related functions, Classes of operating systems, O.S and the computer system, Batch processing system, Multiprogramming systems, Time sharing systems, Real time operating systems, distributed operating systems. Structure of the Operating Systems: Operation of an O.S, Structure of the supervisor, Configuring and installing of the supervisor, Operating system with monolithic structure, layered design, Virtual machine operating systems, Kernel based operating systems, and Microkernel based operating systems.

**Unit II**

Process Management: Process concept, Programmer view of processes, OS view of processes, Interacting processes, Threads, Processes in UNIX, Threads in Solaris. Memory Management: Memory allocation to programs, Memory allocation preliminaries, Contiguous and noncontiguous allocation to programs, Memory allocation for program-controlled data, kernel memory allocation.

**Unit III**

Virtual Memory: Virtual memory basics, Virtual memory using paging, Demand paging, Page replacement, Page replacement policies, Memory allocation to programs, Page sharing, UNIX virtual memory. File Systems: File system and IOCS, Files and directories, Overview of I/O organization, Fundamental file organizations, Interface between file system and IOCS, Allocation of disk space, Implementing file access, UNIX file system.

**Unit IV**

Scheduling: Fundamentals of scheduling, Long-term scheduling, Medium and short term scheduling, Real time scheduling, Process scheduling in UNIX. Message Passing: Implementing message passing, Mailboxes, Inter process communication in UNIX.

**Text Book:**

**Reference Books:**

<table>
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<tr>
<th>Course Title: Advanced Microprocessor</th>
<th>Course Code: UEC617E</th>
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<tr>
<td>Credits: 3</td>
<td>Teaching Hours: 40 Hrs (10 Hrs/Unit)</td>
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<td>Contact Hours: 3 Hrs/Week</td>
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**Unit I**

Embedded processor architecture, IA32 architecture, Micro-architecture, IA32 Instruction set and programming, Floating point format, FPU instructions, MMX instructions, SIMD and SSE family.

**Unit II**

Function Calls, Pointer manipulation, exchange of arguments and results, frame pointers, Interrupts and exceptions.

**Unit III**

Assemblers, directives, Macros, simulation and debugging tools. Hardware interface to various peripherals.

**Unit IV**

Assembly for system initialization, C code optimization using assembly, assembly in Linux kernel, Code generation through compilers. Socket programming.

**Text Books:**

1) Peter Barry & Patrick Crowley, “Modern Embedded Computing”.
2) Lori Matassa & Max Domeika, “Break Away with Intel Atom processors”.

**Reference Books:**

1) Kip R. Irvin, “Assembly Language for x86 Processors”.
2) Jeff Duntemann, “Assembly Language Step-by-Step”.
**Course Title:** Applications of Signal Processing  
**Course Code:** UEC618E  
**Credits:** 3  
**Teaching Hours:** 40 Hrs (10 Hrs/Unit)  
**Contact Hours:** 3 Hrs/Week  
**CIE Marks:** 50  
**SEE Marks:** 50  
**Total Marks:** 100

### Unit I

Analog to digital conversion and concept of digital frequency. Introduction to Z-transform, DFT and its properties, DCT. Linear filtering of long sequence (overlap add and overlap-save methods). Review of common signal processing operations: Convolution, autocorrelation, cross correlation, power spectral density and their applications. Time dependent processing: short time energy and average magnitude, short time average zero crossing detectors.

### Unit II


### Unit III


### Unit IV


### Text Books:


<table>
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<th>Reference Books:</th>
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Course Title: DSP Processors

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<th>Credits: 3</th>
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### Unit I

Introduction to Programmable DSPs: Multiplier and multiplier accumulator (MAC), Modified bus structures and memory access Schemes in P-DSPs, Multiple access memory, Multi-ported memory, VLIW architecture, Pipelining, Special addressing modes in P-DSPs. On-chip peripherals. Computational Accuracy in DSP Implementations: Introduction, Number formats for signals and coefficients in DSP systems, Dynamic range and precision, Sources of error in DSP implementations.

### Unit II

Architecture of DSP Processor-TMS320C5X: Bus structure, Central arithmetic and logic unit (CALU), Auxiliary register ALU, Index register, Auxiliary register compare register, Block move address register, Block repeat registers, Parallel logic unit, Memory mapped registers, Program controller, Flags in the status registers.

TMS320C5X Assembly Language Instructions: Assembly language syntax, Addressing modes, Load/Store instructions, Addition/Subtraction instructions, Move instructions, Multiplication instructions, The NORM instruction.

### Unit III

Instruction Pipelining in TMS320C5X and Programming: Program control instructions, Peripheral control, Pipeline structure, Pipeline operation, Normal pipeline operation, C50-based starter kit (DSK), Programs for familiarization of addressing modes, Programs for familiarization of arithmetic instructions.

### Unit IV

Real Time Signal Processing Using TMS320C5X: On chip timer in C5X and programming its mode, C5X Serial port block diagram and its operation, Analog interfacing circuit (AIC), Terminal functions, Analog input and output, A/D and D/A filters, Internal timing configuration, AIC serial port modes and its registers, AIC serial port operation and reset function, Interfacing the DSP and AIC, FIR filter implementation.

### Text Books:


**Reference Book:**

<table>
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<tr>
<th>Course Title: Mobile Communication</th>
<th>Course Code: UEC620E</th>
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<td>Total Marks: 100</td>
<td>Contact Hours: 3 Hrs/Week</td>
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</tbody>
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### Unit I


### Unit II

Spread Spectrum: The concept of spread spectrum, Frequency hopping spread spectrum, direct sequence spread spectrum, Code division multiple access, Generation of spreading sequences.

### Unit III


### Unit IV

Mobile network layer: Mobile ad-hoc networks, Mobile transport layer: Traditional TCP, Classical TCP improvements, TCP over 2.5/3G wireless networks, Performance enhancing proxies, Support for mobility: File systems, WWW, WAP.

### Text Books:


### Reference Books:

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<td>Total Marks: 100</td>
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**List of Experiments**

1) **Network experiments using C**
   - (a) Simulate bit/ character stuffing and de-stuffing using HDLC.
   - (b) Simulate the shortest path algorithm.
   - (c) Encryption and decryption of a given message.
   - (d) Find minimum spanning tree of a subset.
   - (e) Compute polynomial code checksum for CRC-CCITT

2) **Network experiments using NS2**
   - (a) To create a network topology for three nodes. To create a network topology for a star topology of 12 nodes, to create a topology of 4 nodes for different link capacities and observe the data flow in the network.
   - (b) To simulate the network of 5 nodes and use the routing protocol dynamically and trace the link up and down in between nodes.
   - (c) To simulate a network to perform shortest path routing for a network topology of 9 nodes.
   - (d) To test the operation of multicast routing and trace the packet delivery.
   - (e) To create topology of 7 nodes and observe the data flow at different nodes.

3) **Study of Network programming:**
   - (a) Client server programming using TCP.
   - (b) Client server programming using UDP.
   - (c) Client server programming using TCP and file sharing with semaphores.

4) **Study of wireless LANs, Sensor networks and campus network**
List of Experiments

Design Simulation and Layout for the following

1) Inverter
2) Two input NAND Gate
3) Two input NOR gate
4) Two input XOR / XNOR gates
5) Two input OR gate
6) Two input AND gate
7) NMOS/PMOS transistor VI characteristics
8) NMOS / PMOS and TG as switch
9) D flip flop and T flip flop
10) 3-bit Counter
11) 3-bit Shift Register
12) Full adder
13) Parallel Adder